REMARKS

The following remarks are made in response to the Non-Final Office Action mailed May 21, 2009. Claims 43 and 45 have been withdrawn from consideration. Claims 22-25, 27-37, 39-42, and 44 were rejected. With this Response, claims 22, 41 and 44 have been amended. Claims 22-25, 27-37, 39-42, and 44 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 22, 27, 28, 33, 35, 40-41, and 44 under 35 U.S.C. § 102(e) as being anticipated by the Farnworth et al. U.S. Patent No. 6,515,325. Applicant respectfully disagrees that these claims, as amended, are taught or suggested in the art of record.

As amended, claim 22 is a vertically integrated field-effect transistor including a first electrically conductive layer, a middle layer, formed partially from dielectric material, on the first electrically conductive layer, and a second electrically conductive layer on the middle layer. A nanostructure is ***grown up in a via hole from the bottom of the via hole introduced into the middle layer such that the grown nanostructure does not contact adjacent sidewalls of the via hole***. The nanostructure includes a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer. The first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor. The middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers. A ***thin*** ring structure ***formed by oxidizing the third electrically conductive layer resulting in an oxidized layer as the gate-insulating region*** of the field-effect transistor arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein. This is not taught or suggested.

On page 2 of the Office Action, it is stated that the limitation of "grown up in a via hole from the bottom of the via hole" is considered as "process of making" while the claims are considered as "product by process". In response, Applicant has clarified to recite the specific structural advantage of this recited feature. Using the process of growing up the nanostructure in the via hole results in a nanostructure that has a gap between the side-walls and the nanostructure in the via hole. This is illustrated, for example in Figures 1A and 1B and accompanying description in the specification, between the nanotube 104 and the ring structure 106, labeled as via hole 108.

In contrast to the subject matter claimed in amended claim 22 (as well as 41 and 44), the Farnworth reference does not disclose the nanostructure is grown up in a via hole from the bottom of the via hole. In fact, Farnworth merely discloses (in connection with related embodiments) that an insulating layer is formed (deposited) over a pre-grown nanotube (see col. 5, lines 29 to 34 and FIG. 2G; col. 7, lines 1 to 3 and FIG. 4C).

As is thus evident from the Farnworth reference, using the opposed process, which means that in a first step, the nanostructure is produced and after that the insulating structure is deposited on the nanostructure such that the insulating layer contacts the nanostructure everywhere, leads to the opposed feature of the product. As such, this different process leads to a product that is different from and non-obvious over prior art.

In contrast to the arrangement of Farnworth, nanostructure according to amended claims is grown up in a via hole. Hence, the nanostructure in grown up a via hole as claimed by amended claims results in a region in the via hole between the nanostructure and the respective dielectric sublayer, which is free of electrically insulating material. In contrast thereto, in the field-effect transistor device 70 shown in FIG. 5 of Farnworth, the sub regions of insulating layer 20 above, below and between gates 79 and 81 are formed directly on the nanotube 22. That is, there is no region free of electrically insulating material left in the via hole between nanostructure 22 and the insulating material of layer 20 within regions A, C and E.

In that way, it is possible to implement the nanostructure without the danger of destruction of the nanostructure by a subsequent deposition process as it is the case for the structure disclosed by Farnworth.

Because this feature is not taught or suggested in the art, these claims are in condition for allowance.

Furthermore, claim 22 has been amended to additionally clarify that a ***thin*** ring structure is formed by oxidizing the third electrically conductive layer. Support for the amendment can be found at least in paragraph [0079]. The resulting recited ***oxidized layer*** is also not taught or suggested in the art of record.

Reducing the thickness of the gate-insulating region in this way results in enabling a lower gate-voltage and a higher current through the nanowire, which results in a higher switching-velocity. This reduction of thickness of the gate-insulating region is only possible by oxidation, whereas a gate-insulation layer formed by deposition would be considerably thicker.

Farnworth, Mancesvki and the other art of record fail to describe the additional feature of a thin ring structure formed by oxidizing the third electrically conductive layer as gate-insulating region.

Because independent claims 22, 41 and 44, as well as dependent claims 27, 28, 33, 35, and 40 include these features, they are in condition for allowance. Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 102 rejection to the claims, and request allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325 in view of the Fitch et al. U.S. Patent No. 5,612,563.

The Examiner rejected claims 30-31 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325 in view of the Watanabe et al. U.S. Patent Application Publication No. 2002/0130333.

The Examiner rejected claims 23-25, 36, and 42 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325 in view of the Mancevski U.S. Patent Application Publication No. 2001/0023986.

The Examiner rejected claims 32 and 39 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325.

The Examiner rejected claim 34 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325 in view of the Banin et al. U.S. Patent Application Publication No. 2003/0214699.

The Examiner rejected claim 37 under 35 U.S.C. § 103(a) as being unpatentable over the Farnworth et al. U.S. Patent No. 6,515,325 in view of the Mancevski U.S. Patent Application Publication No. 2001/0023986, and further in view of the Banin et al. U.S. Patent Application Publication No. 2003/0214699.

Because claims 23-25, 36 and 42 are ultimately dependent on one of claims 22, 41 and 44, which are allowable as discussed above, they too are in proper form for allowance. Therefore, Applicant respectfully requests reconsideration and withdrawal of the 35 U.S.C. § 103 rejection to the claims, and request allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 22-25, 27-37, 39-42, and 44 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 22-25, 27-37, 39-42, and 44 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Andrew Graham et al.,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 767-2502
Facsimile: (612) 573-2005

Date: October 21, 2009
PPK:cms

/paulpkempf/
Paul P. Kempf
Reg. No. 39,727